IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Group Art Unit: 2827
Examiner: David A. ZARNEKE

In Re PATENT APPLICATION Of:

Applicant(s): Takaaki SASAKI

Serial No.: 09/942,962

Filed: August 31, 2001

For: SEMICONDUCTOR PACKAGE FOR THREE-DIMENSIONAL MOUNTING, FABRICATION METHOD THEREOF, AND SEMICONDUCTOR DEVICE

Docket No.: TAI-131

AMENDMENT

August 22, 2002

Assistant Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Sir:

In response to the Examiner's Action mailed on May 31, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 14~23 without prejudice or disclaimer to the subject matter recited therein.

Please amend the following claim:

1. (Amended) A semiconductor package for three-dimensional mounting, comprising:

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FEE ENCLOSED:$ None
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a first substrate having an upper surface on which a first metal pattern is formed and a lower surface on which a second metal pattern is formed, said first metal pattern and second metal pattern being electrically connected to each other;

a semiconductor chip which is placed on the upper surface of the first substrate and is electrically connected to the first metal pattern;

a sealing resin layer which is formed on the upper surface of the first substrate and seals the semiconductor chip and the first metal pattern;

a conductive wire which passes through the resin layer and has one end electrically connected to the first metal pattern and the other end exposed at a top surface of the resin layer, the exposed other end of said conductive wire and the top surface of the resin layer being substantially level with each other; and

a first electrode which is formed on the lower surface of the first substrate and is electrically connected to the second metal pattern.

Please add the following claims:

--24. A semiconductor package for three-dimensional mounting, comprising:

a first substrate having an upper surface on which a first metal pattern is formed and a lower surface on which a second metal pattern is formed, said first metal pattern and second metal pattern being electrically connected to each other;

a semiconductor chip which is placed on the upper surface of the first substrate and is electrically connected to the first metal pattern;

a sealing resin layer which is formed on the upper surface of the first substrate and seals the semiconductor chip and the first metal pattern;

a conductive wire which passes through the resin layer and has one end electrically connected to the first metal pattern and the other end exposed at a top surface of the resin layer;

a first electrode which is formed on the lower surface of the first substrate and is electrically connected to the second metal pattern; and

a wiring pattern formed over the sealing resin layer and being electrically connected to the conductive wire, said wiring pattern being comprised of at least a first wiring and a second wiring, said first wiring being disposed closer to a center of the semiconductor package than said second wiring is, and said second wiring being disposed closer toward a periphery of the semiconductor package than said first wiring is.

25. The semiconductor package defined in claim 24, wherein said wiring pattern comprises a plurality of said first wirings, and a plurality of said second wirings, said first wirings and said second wirings being alternatingly arranged.

26. A semiconductor package for three-dimensional mounting, comprising:

a first substrate having an upper surface on which a first metal pattern is formed and a lower surface on which a second metal pattern is formed, said first metal pattern and second metal pattern being electrically connected to each other;

a semiconductor chip which is placed on the upper surface of the first substrate and is electrically connected to the first metal pattern;

a sealing resin layer which is formed on the upper surface of the first substrate and seals the semiconductor chip and the first metal pattern;

a conductive wire which passes through the resin layer and has one end electrically connected to the first metal pattern and the other end exposed at a top surface of the resin layer;

a first electrode which is formed on the lower surface of the first substrate and is electrically connected to the second metal pattern;

(12 a wiring pattern formed over the sealing resin layer and being electrically connected to the conductive wire, said wiring pattern being comprised of Cu; and

a second electrode formed on the wiring pattern, the second electrode including an Ni layer in electrical connection with the wiring pattern, and an Au layer disposed on the Ni layer.

REMARKS

The Examiner's Action mailed on May 31, 2002 has been received and its contents carefully considered.

In this Amendment, Applicant has amended claim 1, canceled claims 14~23 and added claims 24~26. Claims 1, 24 and 26 are the independent claims. Claims 1~13 and 24~26 are pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

The Examiner has rejected claims 1~4, 7, 8, 11 and 12 as being anticipated by *Yamashita et al.* (USP 5,726,493). It is submitted that these claims are patentably distinguishable over the cited reference for at least the following reasons.

Applicant's independent claim 1 has been amended to recite that the conductive wire has an exposed end which is substantially level with a top surface of the resin layer. This claimed configuration results in a structure that allows the solder balls to be stably arranged.

In contrast, *Yamashita et al.* disclose electrode members 17 which have top ends which protrude from a sealing resin 16. This reference discloses that this configuration allows for the electrode members 17 to be electrically connected to outer terminals outside of the sealing resin 16 (see column 6, lines 1-4). Thus, not only does this reference not disclose Applicant's claimed configuration, but this reference specifically teaches away from modifying the electrode members 17 so that the electrode members 17 would have an exposed end which is substantially level with a top of the sealing resin 16. As such, it is submitted that Applicant's independent claim 1, and the claims dependent therefrom, are *prima facie* patentably distinguishable over the cited reference. It is thus requested that these claims be allowed and that this rejection be withdrawn.

The Examiner has further rejected claims 5, 6, 9, 10 and 13 as being obvious over *Yamashita et al.* and further in view of *Aiba et al.* (USP 6,348,728). Because claims 5, 6, 9, 10 and 13 depend from independent claim 1, and because *Aiba et al.* do not overcome the above-noted deficiencies of *Yamashita et al.*, and further in view of the fact that *Yamashita et al.* teach away from modifying the electrode members 17 in a manner similar to the structure required by Applicant's independent claim 1, it is submitted that these claims are patentably distinguishable over the cited references for at least the same reasons as independent claim 1, from which these claims depend, as

well as for the additional features recited therein. It is thus requested that this rejection be withdrawn and that these claims be allowed.

Applicant has further added an independent claim 24 which recites a semiconductor package which has a wiring pattern that includes at least a first wiring and a second wiring. The first wiring is disposed closer to the center of the semiconductor package than the second wiring is. The second wiring is disposed closer toward a periphery of the semiconductor package than the first wiring is. This configuration allows the first wirings to be electrically connected to external terminals at a location that is near to the center of the semiconductor package, and allows the second wirings to be electrically connected to external terminals at a location that is near to peripheral portions of the semiconductor package. Thus, this configuration allows solder balls, for example, to be arranged without contacting one another, which may otherwise cause shorts. In contrast, none of the cited references disclose or otherwise suggest the arrangement of such wiring patterns. Moreover claim 25 recites that the wiring pattern comprises a plurality of the first wirings and a plurality of the second wirings, with the first and second wirings being alternately arranged. This configuration allows the pitch or spacing of the solder balls, for example, to be wider than a conventional arrangement pattern. In contrast, none of the cited references disclose or otherwise suggest this feature. It is thus requested that these claims be allowed.

Further, independent claim 26 recites that a wiring pattern is provided which is comprised of Cu, and a second electrode is formed on the wiring pattern with the second electrode including an Ni layer in electrical connection with the wiring pattern,

and an Au layer disposed on the Ni layer. In this structure, the Ni layer prevents inter-diffusion of Cu in the wiring pattern and Au in the second electrode. In contrast, neither of the cited references disclose or otherwise suggest these features. It is requested that this claim be allowed.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of the application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

August 22, 2002
Date

Robert H. Berdo, Jr.
RABIN & BERDO
Registration No. 38,075
Customer No. 23995
Telephone: 202-371-8976
Facsimile: 202-408-0924

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